

AMIBIOS

- D0 The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
- D1 Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
- D3 Starting memory sizing next.
- D4 Returning to real mode. Executing any OEM patches and setting the stack next.
- D5 Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
- D6 Control is in segment 0. Next, checking if <Ctrl><Home> was pressed and verifying the system BIOS checksum.
If either <Ctrl><Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h.
Otherwise, going to checkpoint code D7h.
- E0 The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
- E1 Initializing the interrupt vector table next.
- E2 Initializing the DMA and Interrupt controllers next.
- E6 Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
- Ed Initializing the floppy drive.
- Ee Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
- Ef A read error occurred while reading the floppy drive in drive A:.
- F0 Next, searching for the AMIBOOT.ROM file in the root directory.
- F1 The AMIBOOT.ROM file is not in the root directory.
- F2 Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
- F3 Next, reading the AMIBOOT.ROM file, cluster by cluster.
- F4 The AMIBOOT.ROM file is not the correct size.
- F5 Next, disabling internal cache memory.
- FB Next, detecting the type of flash ROM.
- FC Next, erasing the flash ROM.
- FD Next, programming the flash ROM.
- FF Flash ROM programming was successful. Next, restarting the system BIOS.
- 03 The NMI is disabled. Next, checking for a reset or a power on condition.
- 05 The BIOS stack has been built. Next, disabling cache memory.
- 06 Uncompressing the POST code next.

- 07 Next, initializing the CPU and the CPU data area.
- 08 The CMOS checksum calculation is done next.
- 0A The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
- 0B The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued.
- 0C The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
- 0E The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
- 0F The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
- 10 The keyboard controller command byte is written. Next, issuing the Pin12 and 24 blocking and unblocking command.
- 11 Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
- 12 Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
- 13 The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
- 14 The 8254 timer test will begin next.
- 19 The 8254 timer test is over. Starting the memory refresh test next.
- 1A The memory refresh line is toggling. Checking the 15 second on/off time next.
- 23 Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BOIS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
- 24 The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.
- 25 Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
- 27 Any initialization before setting video mode will be done next.
- 28 Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode setting next.
- 2A Bus initialization system, static, output devices will be done next, if present. See page 6 for additional information.
- 2B Passing control to the video ROM to perform any required configuration

- before the video ROM test.
- 2C All necessary processing before passing control to the video ROM is done.
Looking for the video ROM next and passing control to it.
- 2D The video ROM has returned control to BOIS POST.Performing any
required processing after the video ROM had control.
- 2E Completed post-video ROM test processing.If the EGA/VGA controller is
not found, performing the display memory read/write test next.
- 2F The EGA/VGA controller was not found.The display memory read/write
test is about to begin.
- 30 The display memory read/write test passed.Look for retrace checking next.
- 31 The display memory read/write test or retrace checking failed.Performing
the alternate display memory read/write test next.
- 32 The alternate display memory read/write test passed.Looking for alternate
display retrace checking next.
- 34 Video display checking is over.Setting the display mode next.
- 37 The display mode is set.Displaying the power on message next.
- 38 Initializing the bus input,IPL,general device next, if present. See page 6 for
additional information.
- 39 Displaying bus initialization error messages.See page 6 for additional
information.
- 3A The new cursor position has been read and saved.Displaying the Hit
message next.
- 3B The Hitmessage is displayed.The protected mode memory test is
about to start.
- 40 Preparing the descriptor tables next/
- 42 The descriptor tables are prepared Entering protected mode for the memory
test next.
- 43 Entered protected mode.Enabling interrupts for diagnostic mode next.
- 44 Interrupts enabled if the diagnostics switch is on.Initializing data to check
memory wraparound at 0:0 next.
- 45 Data initialized. Checking for memory wraparound at 0:0 and finding the
total system memory size next.
- 46 The memory wraparound test is done.Memory size calculation has been
done.Writing patterns to test memory next.
- 47 The memory pattern has been written to extended memory.Writing patterns
to the base 640 KB memory next.
- 48 Patterns written in base memory.Determining the amount of memory below
1 MB next.

49 The amount of memory below 1 MB has been found and verified.
Determining the amount of memory above 1 MB memory next.

4B The amount of memory above 1 MB has been found and verified. Checking
for a soft reset and clearing the memory below 1 MB for the soft reset next.
If this is a power on situation, going to checkpoint 4E next.

4C The memory below 1 MB has been cleared via a soft reset. Clearing the
memory above 1MB next.

4D The memory above 1MB has been cleared via a soft reset. Saving the
memory size next. Going to checkpoint 52 next.

4E The memory test started, but not as the result of a soft reset. Displaying the
first 64 KB memory size next.

4F The memory size display has started. The display is updated during the
memory test. Performing the sequential and random memory test next.

50 The memory below 1MB has been tested and initialized. Adjusting the
displayed memory size for relocation and shadowing next.

51 The memory size display was adjusted for relocation and shadowing. Testing
the memory above 1MB next.

52 The memory above 1 MB has been tested and initialized. Saving the memory
size information next.

53 The memory size information and the CPU registers are saved. Entering real
mode next.

54 Shutdown was successful. The CPU is in real mode. Disabling the Gate A20
line, parity, and the NMI next.

57 The A20 address line, parity, and the NMI are disabled. Adjusting the
memory size depending on relocation and shadowing next.

58 The memory size was adjusted for relocation and shadowing. Clearing the
Hitmessage next.

59 The Hitmessage is cleared. The<WAIT....>message is displayed.
Starting the DMA and interrupt controller test next.

60 The DMA page register test passed. Performing the DMA Controller 1 base
register test next.

62 The DMA controller 1 base register test passed. Performing the DMA
controller 2 base register test next.

65 The DMA controller 2 base register test passed. Programming DMA
controllers 1 and 2 next.

66 Completed programming DMA controllers 1 and 2. Initializing the 8259
interrupt controller next.

67 Completed 8259 interrupt controller initialization.

- 7F Extended NMI source enabling is in progress.
- 80 The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
- 81 A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
- 82 The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
- 83 The command byte was written and global data initialization has completed. Checking for a locked key next.
- 84 Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
- 85 The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
- 86 The password was checked. Performing any required programming before WINBIOS Setup next.
- 87 The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
- 88 Returned from WINBIOS Setup and cleared the the screen. Performing any necessary programming after WINBIOS Setup next.
- 89 The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
- 8B The first screen message has been displayed. The<WAIT...>message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
- 8C Programming the WINBIOS Setup options next.
- 8D The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
- 8F The hard disk controller has been reset. Configuring the floppy drive controller next.
- 91 The floppy drive controller has been configured. Configuring the hard disk drive controller next.
- 95 Initializing the bus option ROMs from C800 next. See page 6 for additional information.
- 96 Initializing before passing control to the adaptor ROM at C800.
- 97 Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
- 98 The adaptor ROM had control and has now returned control to BIOS POST.

Performing any required processing after the option ROM returned control.

99 Any initialization required after the option ROM test has completed.

Configuring the timer data area and printer base address next.

9A Set the timer and printer base addresses. Setting the RS-232 base address next.

9B Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.

9C Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.

9D Coprocessor initialized. Performing any required initialization after the Coprocessor test next.

9E Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.

A2 Displaying any soft errors next.

A3 The soft error display has completed. Setting the keyboard typematic rate next.

A4 The keyboard tapematic rate is set. Programming the memory wait states next.

A5 Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.

A7 NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E0004 next.

A8 Initialization before passing control to the adaptor ROM at E000 completed. Passing control to the adaptor ROM at E000 next.

A9 Returned from adaptor ROM at E000 control. Performing any initialization required after the E000 option ROM had control next.

Aa Initialization after E000 option ROM control has completed. Displaying the system configuration next.

Ab Uncompressing the DMI data and executing DMI POST initialization next.

B0 The system configuration is displayed.

B1 Copying any code to specific areas.

00 Code copying to specific areas is done. Passing control to INT 19 boot loader next.

2A Initializing the different bus system, static, and output devices, if present/

38 initialized bus input, IPL, and general devices, if present.

39 Displaying bus initialization error messages, if any.

95 Initializing bus adaptor ROMs from C8000 through D8000.